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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,395	11/26/2001	Sergey D. Lopatin	039153-0457 (G1162)	7882

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EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/994,395	LOPATIN ET AL.	
	Examiner	Art Unit	
	Thomas J. Mage	2811	

-- Th MAILING DATE of this communication app ars on the cov r sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *5* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, and 6-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Cancellations

1. Applicant's cancellation of Claim 5 in Letter of January 15, 2004 is acknowledged.

Claim Rejections – 35 U.S.C. 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 4, and 6 - 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. (US 6,030,895) in view of Edelstein et al. (US 6,399,496 B1), and Merchant (US 6,440,849 B1).

4. Regarding Claim 1, Joshi et al. disclose a method for fabricating an interconnection structure used on a device in an integrated circuit wherein a barrier layer (34,40) (Figure 2) (Col. 4, lines 50 – 62) is formed along the lateral sidewalls and bottom of a via aperture, where the via aperture is configured to receive a via material that connects a first and second conductive layer. Joshi et al. further disclose that the via material is subsequently deposited (Col. 8, lines 5 – 8) and comprises a ternary Cu alloy (Col. 8,

lines 24 – 27). Joshi et al. do not disclose the constituents of the ternary alloy. Edelstein et al. disclose that the ternary alloy (Col. 8, lines 49 – 52) can be formed using Cu, Zn (Col. 8, lines 42 – 45) and Cr (Col. 8, lines 35 – 41) and formed in a via. Neither Joshi et al. nor Edelstein et al. disclose that Cr additions to the copper alloy increase and subsequently stabilize the grain size. Merchant et al. disclose that Cr additions to the copper produce an initial increase and subsequent stabilization of grain size (Col. 2, lines 8 – 15). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Merchant et al. and Edelstein et al. with Joshi et al. to provide a stable Cu alloy layer with improved electromigration properties.

5. Regarding Claim 2, Joshi et al. do not disclose that the copper alloy via material includes Ag. Edelstein et al. disclose the use of Ag as an alloying element for Cu. (Col. 8, lines 42 – 45). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Edelstein et al. with Joshi et al. to provide a stable Cu alloy layer with improved electromigration properties.

6. Regarding Claim 3, Joshi et al. do not disclose that the copper alloy via material includes Zn. Edelstein et al. disclose the use of Zn as an alloying element for Cu. (Col. 8, lines 42 – 45). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Edelstein et al. with Joshi et al. to provide a stable Cu alloy layer with improved electromigration properties.

7. Regarding Claim 4, Joshi et al. do not disclose that the copper alloy via material includes one atomic percent of Ag. Merchant et al. disclose that the alloy includes Ag (Col. 3, line 6) and that the concentration is less than one atomic percent (Col. 3, lines 11 – 12). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Merchant et al. with Joshi et al. to provide a stable Cu alloy layer with improved electromigration properties.

8. Regarding Claim 6, Joshi et al. do not disclose that the copper alloy via material includes Cr. Edelstein et al. disclose the use of Cr as an alloying element for Cu. (Col. 8, lines 35 – 41). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Edelstein et al. with Joshi et al. to provide a stable Cu alloy layer with improved electromigration properties.

9. Regarding Claims 7 and 8, Joshi et al. do not disclose that the element for increasing grain size is Cr. Merchant et al. disclose that the element for increasing and stabilizing grain size (Col. 2, lines 8 – 15) is Cr (Col. 3, line 6) and that the concentration is less than one atomic percent (Col. 3, lines 11 – 12). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Merchant et al. and Edelstein et al. with Joshi et al. to provide a stable Cu alloy layer with improved electromigration properties.

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. in

view of Edelstein et al. and Merchant et al., as applied to Claims 1 – 4, and 6 – 8, and further in view of Gross (US 6,380,083 B1).

11. Regarding Claim 9, Joshi et al. do not disclose the grain size of the copper layer (after annealing). Gross discloses that the grain size increases to sizes greater than or equal to 2 um (Col. 5, lines 30 – 36). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Joshi et al. with Gross to obtain copper layers of stable grain size for improved device performance.

12. Claims 10 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. in view of Andricacos et al. (US 6,090,710) and Merchant.

13. Regarding Claim 10, Joshi et al. disclose a method of using a ternary copper alloy (Col. 8, lines 24 – 27) to obtain interconnect or via structures in which a first conductive layer (M1) (Figure 2) is provided over an integrated circuit substrate, followed by the formation of a conformal layer at the bottom and sides of a via aperture to form a barrier layer separating the via from the first conductive layer. Further, Joshi et al. disclose that the via aperture is filled with copper alloy to form a ternary via and a second conductive layer (M2) formed over the via, electrically connecting first and second conductive layers.

Joshi et al. do not explicitly disclose that the addition of select alloying elements

will yield low resistance within the copper vias. However, Andricacos et al. disclose (Col. 8, Table 1) that the resistivity of copper alloys containing one percent or less of Sn and other alloying elements is altered. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Andricacos et al. with Joshi et al. to obtain low resistance (resistivity) copper alloys for vias.

Further, Joshi et al. do not disclose the presence of Cr or Ca. However, Merchant et al. disclose the addition of Cr element to the copper alloy for grain size control. It would have been obvious to one of ordinary skill in the art at the time of the invention to add the element Cr for grain size control and thus to combine Joshi et al. and Merchant et al.

14. Regarding Claim 11, Joshi et al. do not disclose a ternary copper alloy via material containing at least 98 percent copper. Andricacos et al. disclose that the addition of an alloying element in the range, 0.01 and about 2 weight percent (Col. 8, lines 15 – 16) with at least 98 percent Cu.

15. Regarding Claim 12, Joshi et al. do not disclose that the ternary copper alloy via includes Sn. Andricacos et al. disclose (Col. 8, Table 1) that Sn is included in the via. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Andricacos et al. with Joshi et al. to obtain low resistance (resistivity) copper alloys for vias.

16. Regarding Claims 13 – 16, Joshi et al. do not disclose that the ternary copper alloy via includes one atomic percent or less of an element for increasing grain size or that the element is Cr. Merchant disclose that the element for increasing and stabilizing grain size (Col. 2, lines 8 – 15) is Cr (Col. 3, line 6) and that the concentration is less than one atomic percent (Col. 3, lines 11 – 12). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Merchant et al. with Joshi et al. to provide a stable Cu alloy layer with improved electromigration properties.

17. Claims 17 - 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. in view of Edelstein et al.

18. Regarding Claims 17 and 19, Joshi et al. disclose a method of forming a via in an integrated circuit, wherein a first conductive layer (M1) (Figure 2) is formed, followed by deposition of an etch stop layer (34) over the first conductive layer and an insulating layer (14) over the etch stop layer, whereupon, an etch is applied and an aperture formed in the insulating layer and etch stop layer. Joshi et al. further disclose that a barrier material (40,34) is provided at the bottom and sides of the aperture, followed by a fill of the aperture with a ternary (Col. 8, lines 24 – 27) Cu alloy and formation of a second conducting line (M2), where the via electrically connects the first and second conductive layers.

Joshi et al. do not disclose the constituents of the Cu alloy. Edelstein et al. disclose that a ternary alloy (Col.8, lines 49 – 52) can be formed using Cu, Zn (Col. 8, lines 42 – 45) and Cr (Col. 8, lines 35 – 41) and formed in a via. It would have been obvious to one of ordinary skill in the art at the invention to use the procedures of Edelstein et al. in Joshi et al. to obtain a filled via with a combination of improved electromigration resistance, adhesion, and surface properties (Edelstein et al., Col. 8, lines 51 – 52)

19. Regarding Claims 18 and 20, Joshi et al. do not disclose a copper alloy material that includes Cu, Sn, and Ca or that the compound source includes CuAgCr and CuSnCa. Edelstein et al. disclose that a ternary copper alloy (Col. 8, lines 49 – 52) can be formed comprising the following: CuAgCr (Col.8, lines 35 – 45) and CuSnCa (Col. 8, lines 31 – 41). It would have then been obvious to one of ordinary skill in the art at the time of the invention to use the ternary alloy of Edelstein et al. in Joshi et al. to obtain a filled via with a combination of electromigration resistance, adhesion, and surface properties (Edelstein et al., Col. 8, lines 51 – 52).

20. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al., in view of Edelstein et al. as applied to Claims 17 – 20 above, and further in view of Merchant et al.

21. Regarding Claims 21 and 22, Joshi et al. do not disclose that the element for increasing grain size is Cr or the stuffing of grain boundaries. Merchant et al. disclose that the element

for increasing and stabilizing grain size (Col. 2, lines 8 – 15) is Cr (Col. 3, line 6) and that the concentration is less than one atomic percent (Col. 3, lines 11 – 12). Further, Merchant et al. disclose (Col. 2, line 62 through Col. 3, line 3) the motion of dopant or alloy element to grain boundaries to produce pinning and "stuffing" of grain boundaries. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Merchant et al. and Edelstein et al. with Joshi et al. to provide a stable Cu alloy layer with improved electromigration properties.

22. Claim 23. is rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al., in view of Edelstein et al. as applied to Claims 17 – 20 above, and further in view of Gross.

23. Regarding Claim 23, Joshi et al. do not disclose the grain size of the copper layer (after annealing). Gross discloses that the grain size increases to sizes greater than or equal to 2 um (Col. 5, lines 30 – 36). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Joshi et al. with Gross to obtain copper layers of stable grain size for improved device performance.

Response to Arguments

15. Applicant's arguments with regard to claim rejections have been carefully considered but these have been found to be unpersuasive. It should be remarked that Edelstein et al. use a deposition procedure to form a stable copper alloy within a via where the layer is formed by sputtering, ionized sputtering, CVD, evaporation and electrochemical

means, analogous to procedures recited in the instant application. It is irrelevant that the layer deposited is a "seed layer" or whether or not this is "filled" to the top of the via, since the claim limitations have no such restriction.

Conclusions

16. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee
April 14, 2004